Japanese Patent Laid-Open No. 62-185471

Specification

Title of the Invention

Solid-State Image Pickup Device

Claim for the Patent

A solid-state image pickup device comprising photoelectric conversion devices arranged in a two-dimensional array, vertical switch means for selecting the photoelectric conversion devices, a vertical signal line which connects an output terminal of each of the vertical switch means with one another for each column, and horizontal switch means for selecting the vertical signal line, characterized by comprising: switch means for resetting potential of a vertical signal line for each vertical signal line; amplification means for detecting and amplifying potential of the vertical signal line between the vertical signal line and the horizontal switch means; and means for outputting a difference between blank vertical signal line potential after the reset and potential of a vertical signal line having signal charge.

Detailed Description of the Invention

[Field of Application of the Invention]

The present invention relates to a solid-state image pickup device, and more specifically to a suitable configuration for realizing high sensitivity and low smear, and a control method thereof in a MOS solid-state image pickup device.

[Background of the Invention]

Conventionally, a MOS solid-state image pickup device is well known as a type of two-dimensional solid-state image pickup device (by Aoki, ISSCC Digest, p26, 1980). Figure 1 shows an example of a conventional circuit configuration of the MOS solid-state image pickup device. Photoelectric conversion devices 1 are arranged in a two-dimensional array. Vertical scanning circuit 3 and horizontal scanning circuit 5 are for sequentially reading the signal charge in the photoelectric conversion devices. A vertical switch 2 is turned on and off by the pulse of

the vertical scanning circuit. A vertical gate line 9 transmits the pulse of the vertical scanning circuit to each vertical switch. A horizontal switch 6 is turned on and off by the pulse of the horizontal scanning circuit. Reference numeral 4 designates a vertical signal line. An amplifier 7 is external to the device. Reference numeral 8 designates a horizontal signal line. In this circuit, the signal charge of the photoelectric conversion device 1 is transmitted to the vertical signal line 4 when the vertical switch 2 selected by the vertical scanning circuit 3. Then, the horizontal switch 6 is sequentially opened and closed by the horizontal scanning circuit 5, and the signal charge is read from the amplifier 7 through the horizontal signal line 8.

The device has an advantage of a high photo usage rate and a large amount of signal charge, but has the two following problems. First, there is large random noise occurring when a signal is read, and the signal to noise ratio (hereinafter referred to as an S/N) is low at low illumination. Furthermore, when an image of bright illuminated subject is taken, a vertical smear phenomenon occurs in which long white trails vertically appear on a regenerated image, thereby causing degradation in image quality when an image is taken under a high illumination condition.

[Object of the Invention]

The present invention aims at providing a high S/N and low smear solid-state image pickup device while maintaining a high optical use rate of a MOS solid-state image pickup device, and reducing the random noise and the smear.

[Summary of the Invention]

There are two main components of the random noise of a MOS solid-state image pickup device, that is, the noise generated by a horizontal switch and the noise generated by an amplifier external to the device. The first noise generated by the horizontal switch is essentially generated by the same mechanism as the reset noise generated in an FDA (floating diffusion amplifier) circuit normally used in a CCD (charge coupler device). That is, when the

horizontal switch is turned on/off, a signal is read, and the vertical signal line potential is reset, the reset potential of the vertical signal line is fluctuated by the thermal noise of the horizontal switch, thereby causing random noise. In the FDA circuit, a correlation duplex sampling method is used to reduce the reset noise (M. H. WHITE et al.: IEEE J. Solid State Circuits, vol. SC-9 No. 1 P1-P12 (FEB. 1984): Nishida et al: National Convention of the Institute of Television Script 3-2 p45 (1985): Endoh et al: National Convention of the Institute of Television Script 3-5 p51 (1985)). The present invention notes that the noise generated by the horizontal switch is generated by the same mechanism as the reset noise of the FDA circuit, and provides an amplifier and a circuit for performing the correlation duplex sampling method for each vertical signal line of a MOS image pickup device, thereby reducing the noise occurring by the horizontal switch. Furthermore, as a result of providing the amplifier for each vertical signal line, the noise of the amplifier as another large noise source of the conventional device can be reduced because, first, the capacitance at the input terminal of the amplifier is reduced as compared with the conventional device to realize a large signal amplitude, and second, the pass band required for the amplifier can be reduced.

The smear phenomenon in the MOS image pickup device occurs by unnecessary charge entering the vertical signal line. In the present invention, after resetting the vertical signal line, a true signal charge is read, thereby shortening the smear entering time and reducing the smear.

[Embodiments of the Invention]

The first embodiment of the present invention is described below with reference to Figures 2 and 3. Figure 2 shows the configuration of the circuit according to an embodiment of the present invention. Reference numerals 1 to 6 and 9 are the same as those shown in Figure 1. An amplification circuit 21 detects and amplifies the potential of each vertical signal line. Switches 22 and 23 sample and hold the output of the amplifier 21. Capacitances 27 and 28 are used for sample-and-hold. A differential amplifier 24 outputs a difference between two

sampled and held signals. A reset switch 25 resets a vertical signal line. A reset drain 26 supplies a reset voltage of the vertical signal line. Figure 3 shows pulse timing for drive of the devices shown in Figure 2. An HBL indicates a horizontal blanking interval, and RG, 31, S2 indicate the voltages applied to the respective terminals shown in Figure 2. Described below are the operations of the present embodiment.

In the horizontal blanking interval, RG indicates a high level. When the reset switch 25 is opened, the pseudo signal such as smear charge etc. accumulated in the vertical signal line is swept into the reset drain 26, and the vertical signal line potential is reset to the voltage RD of the reset drain 26 (t_1 in Figure 3). When RG indicates a low level, the thermal noise of the reset switch 25 generates a noise voltage vn, and the reset voltage of the vertical signal line fluctuates (t_2 in Figure 3). The noise voltage vn is amplified by the amplifier 21 (gain: G_1), and when the switch 23 is opened/closed, it is sampled and held as the potential fluctuation of G_1 vn in the capacitance 28 (t_3 in Figure 3).

Afterwards, when the potential V_p of a vertical gate line 9 selected by the vertical scanning circuit 3 becomes high, the vertical switch 2 is opened, and the signal charge Qs is read to the vertical signal line 4 from the photoelectric conversion device 1 (t_4 in Figure 3). The potential fluctuation vs + vn of the vertical signal line obtained by superposing the noise voltage vn to the vertical signal line potential fluctuation vs = Qs/C_v (C_v indicates the capacitance of the vertical signal line) caused by the signal charge is amplified by the amplifier 21, and sampled and held as the potential fluctuation of G_1 (vs + vn) in the capacitance 27 if the switch 22 is opened/closed (t_5 in Figure 3). After the operations above, the potential fluctuation vs of the vertical signal line by the true signal charge without the reset voltage vn of the vertical signal line is amplified by G_1G_2 (G_2 indicates the gain of the differential amplifier 24) and output to the output terminal of the differential amplifier 24. Afterwards, the horizontal scanning circuit 5 sequentially

opens/closes the horizontal switch 6, and an amplified signal is output.

In the embodiment above, the main noise source is the noise generated by the amplifier 21 because, since the signal is amplified by the amplifier 21, the noise of the sample-and-hold circuit and the noise of the differential amplifier 24 can be designed to be ignorable if the voltage gain of the amplifier 21 is large. On the other hand, the necessary operation speed for the amplifier 21 can be the speed at which the sample-and-hold can be sufficiently performed in the capacitances 27 and 28. As a result, the pass band of the amplifier 21 can be as low as 1 MH or less while the pass band of the conventional MOS device is about 3 MHZ, thereby easily reducing the noise.

Since the amount of smear charge entering the signal is differential output, the entering time corresponds to the time period between the closing of the switch 23 and the closing of the switch 22 (T in Figure 3). Therefore, while the smear enters during one horizontal scanning interval in the conventional MOS device, the entering time can be reduced to about 1/30 of the interval, thereby successfully realizing low smear.

In the present embodiment, since the amplifiers 21 and 24 are arranged in parallel by the number of pixels in the horizontal direction, there can be the problem of power consumption. In such a case, lower power consummation can be realized by the pulse operation of each amplifier.

As described above, according to the present embodiment, the random noise and smear can be reduced while maintaining a high optical use rate without making any changes to the photoreceiver of the MOS device.

Next, the second embodiment of the present invention is described below with reference to Figures 4 and 5. In the embodiment shown in Figure 2, it may be difficult to set the operation point of each amplifier in a high gain area because each amplifier is DC-coupled. To solve the above-mentioned problem, a self-bias switch (Nakaya et al: Convention of the Institute of Electronics in 1985 Script 444 p2-162 (1985)) widely used in a MOS A/D converter is used in the present embodiment.

Figure 4 shows the configuration of the circuit according to the second embodiment of the present invention.

In Figure 4, reference numerals 1 to 6 and 9 are the same as those shown in Figure 1. An amplification circuit 41 detects and amplifies the potential of each vertical signal line. A self-bias switch 42 sets the amplification circuit 41 in a high gain area. Reference numeral 43 designates coupling capacitance. Reference numeral 44 designates a second amplification circuit. A self-bias switch 45 sets the amplification circuit 44 in a high gain area. A switch 46 samples and holds a signal. An amplifier 47 outputs a signal. Figure 5 shows a pulse timing for driving the device shown in Figure 4. HBL indicates a horizontal blanking interval, and S1, S2, and S3 indicate voltages at the corresponding terminals shown in Figure 4. Described below are the operations of the present embodiment.

In the horizontal blanking interval, the switch 42 opens, the vertical signal line 4 is reset, and the operation point of the amplifier 41 is set in a high gain area (t_1 in Figure 5). Afterwards, when the switch closes, a noise voltage occurs in a vertical signal line. However, since the switch 45 opens at this time, the output voltage of the amplifier 44 is set at a constant voltage independent of the vertical signal line voltage (t_2 in Figure 5). Next, the switch 45 closes, and the operation point of the amplifier 44 is set in a high gain area. Afterwards, when the potential vp of the vertical gate line 9 selected by the vertical scanning circuit 3 becomes high, the vertical switch 2 opens, and the signal charge is read to the vertical signal line 4 by the photoelectric conversion device 1 (t_2 in Figure 5). After the amplifier 41 amplifies the potential fluctuation of the vertical signal line by the charge, the fluctuation appears at the input terminal of the amplifier 44 through the coupling capacitance 43, and is further amplified by the amplifier 44. By sampling and holding the output of the amplifier 44 at this time, only the output obtained by amplifying the potential fluctuation of the vertical signal line by the signal charge can be sampled and held (t_3 in Figure 5).

Afterwards, the horizontal scanning circuit 5 operates, and the horizontal switch 6 sequentially opens and closes, thereby sequentially outputting a signal through the amplifier 47.

Also in the present embodiment, the random noise suppression effect and the smear suppression effect similar to Figure 2 can be obtained. Furthermore, the present embodiment has an advantage that, since the operation point of the direct current of each amplifier is set by a self-bias, the amplifier can be operated in a high gain area.

The third embodiment of the present invention is described below with reference to Figures 6 and 7. In the embodiment shown in Figure 4, the noise of the amplifier 41 is the main noise source. Therefore, by sufficiently limiting the band of the output of the amplifier 41, the noise can be reduced. The present embodiment adds a charge transfer circuit to the output terminal of the amplifier 41 in order to limit the band.

Figure 6 shows the configuration of the circuit according to the third embodiment of the present invention. The reference numerals 1 to 6, 9, and 41 to 47 are the same as those shown in Figure 4. A transfer gate 61 transmits the output voltage of the amplifier 41 to capacitance 62. A drain 63 inputs a charge to the capacitance 62. An amplifier 64 detects the potential of the capacitance 62. Figure 7(a) shows the pulse timing for drive of the device shown in Figure 6. HBL indicates a horizontal blanking interval. S1, S2, S3, and CI indicate voltages applied to the respective corresponding terminals shown in Figure 6. The operation of the device is almost same as the operation shown in Figure 4. Only the difference is the operation of the low pass filter of charge transfer type configured by the components 61 to 64. The operation is described below with reference to Figure 7(b).

Figure 7(b) shows the potential at the gate 61, the drain 63, and the capacitance 62 at time t_1 and t_2. The output voltage V_0 of the amplifier 41 is the gate voltage of the gate 61. Therefore, the potential at the gate 61 is V_0 - vth. vth indicates the threshold voltage of the gate

61. If the voltage of the drain 63 is changed from a low level to a high level at this time, the charge flows from the capacitance 62 to the drain 63 (Figure 7(b) $t=t_1$). At the transfer ending time, the potential of the capacitance 62 is V_0 - vth (Figure 7(b) $t=t_2$). By detecting the potential of the capacitance 62 by the amplifier 64, the potential fluctuation of the vertical signal line can be read. By analyzing the noise in the circuit, only the component of the frequency band of the reciprocal $1/t_1$ of the charge transfer time t_1 in the noise of the amplifier 41 can contribute to the fluctuation of the voltage of the capacitance 62. That is, the present circuit can operate as a low pass filter for the noise of the amplifier 41.

As described above, the charge transfer circuit functions as a low pass filter in the present embodiment, and the pass band of the amplifier 41 can be limited, thereby easily reducing the random noise.

The fourth embodiment of the present invention is described below with reference to Figures 8 and 9. In a single plate color solid-state image pickup device, there is a vertical two pixel reading scheme in which interlaced scanning is carried out as a method of realizing high quality images with high resolution. In addition, as means for reducing smear, there is a smear differentiation scheme described by Ozawa et al., National Convention of the Institute of Television in 1984, Script 3-13 p67. The present embodiment is an example of realizing these methods by the present invention.

Figure 8 shows the configuration of the circuit according to the fourth embodiment of the present invention. Reference numerals 1 to 6, 9, 41 to 47 are the same as those shown in Figure 4. However, the vertical scanning circuit 3' is provided with a circuit for performing interlaced scanning for simultaneously reading two lines, and three units of the switches 46 for sample-and-hold, the amplifiers 47 for output of a signal, and the horizontal switches 6 are connected for each vertical signal line, and three output lines are provided. Figure 9 shows the pulse timing for drive of the device. HBL indicates a horizontal blanking interval, and S1, S2, S3, S4, and S5 show voltages

applied to the corresponding terminals shown in Figure 8. Described below is the operation according to the present embodiment.

In the present embodiment, the smear signal is read for sample-and-hold to the capacitance 48-1 in the first period (T_1 in Figure 9) of the horizontal blanking interval. The read amount of smear is the amount entering the vertical signal line in the time T_4 until the switch 3 opens and closes again after the switch S2 closes. In the next period (T_2 in Figure 9), the first signal is read for sample-and-hold to the capacitance 48-2. In the final period (T_3 in Figure 9), the second signal is read to the capacitance 48-3 for sample-and-hold. Afterwards, when the horizontal scanning circuit 5 operates, and horizontal switch 6 opens and closes sequentially, the smear charge and the two signal charges are simultaneously read. By subtracting the smear charge from the two signal charges, the signal charge of the vertical two pixels without the smear charge can be obtained.

As described above, in the present embodiment, plural sample-and-hold circuits and output circuits are arranged for each vertical signal line, thereby realizing the smear differential method of easily reading two lines simultaneously.

The fifth embodiment of the present invention is described below with reference to Figures 10 and 11. When strong light is applied to a solid-state image pickup device, the photoelectric conversion device 1 is saturated, the excess charge flows to the vertical signal line 4, and there are pseudo signals appearing as white belts at the top and bottom portions to which the strong light is applied, which degrades the quality of images as with the smear phenomenon. This is called a blooming phenomenon. As means for suppressing the phenomenon, there is an RAB circuit described in the Japanese Utility Model Application No. 55-130240. The present embodiment realizes the RAB circuit according to the present invention.

Figure 10 shows the configuration of the circuit according to the fifth embodiment of the present invention. The reference numerals 1 to 6, 9, and 41 to 47 are the

same as those shown in Figure 4, reference numerals 101 and 102 are a gate and its drain of the RAB circuit for suppressing the blooming. Figure 11 shows the drive pulse timing of the device. Described below is the operations of the present embodiment.

In the horizontal blanking interval, a voltage is applied to the gate 101 of the RAB circuit, and then a low voltage is applied to the drain 102 to slightly open the vertical switch 2. As a result, a part of the charge of the saturated photoelectric conversion device 1 flows to the vertical signal line 4. Then, voltages applied to the drain 102 and the gate 101 of the RAB circuit is lowered in this order and the vertical switch 2 is closed. As a result, in the signal reading period, the photoelectric conversion device 1 is in the state before saturation, thereby incurring no blooming phenomenon. The charge that flows to the vertical signal line 4 is swept to the outside of the device. The subsequent operations are the same as those shown in Figure 4.

As described above, a part of the charge of a saturated photoelectric conversion device is swept to the outside of the device immediately before reading the signal from the photoelectric conversion device 1 according to the present embodiment, and the photoelectric conversion device 1 can be made a unsaturated state, thereby successfully suppressing the blooming phenomenon.

[Advantages of the Invention]

According to the present invention, random noise can be reduced without making any changes to the photoreceiving unit of the MOS solid-state image pickup device, and the time of the smear charge entering a signal can be shortened.

Therefore, a solid-state image pickup device of a high S/N and low smear can be realized.

Brief Description of the Drawings

Figure 1 shows the configuration of the circuit of a conventional solid-state image pickup device. Figures 2, 4, 6, 8, and 10 show the embodiments of the present invention.

Figures 3, 5, 7, 9, and 11 show the timing of the drive pulse.

1 ... photoelectric conversion device, 2 ... vertical

switch, 3 ... vertical scanning circuit, 4 ... vertical signal line, 5 ... horizontal scanning circuit, 6 ... horizontal switch, 9 ... vertical gate line, 21, 41, and 44 ... amplifier, 22, 23, and 46 ... sample-and-hold switch, 24 ... differential amplifier, 47 ... output amplifier, 25 ... reset switch, 26 ... reset drain, 27 and 28 ... sample-and-hold capacitance, 42 and 45 ... self-bias switch, 43 ... coupling capacitor, 61 ... transfer gate, 63 ... charge input drain, 101 ... RAB circuit gate 101, 102 ... RAB circuit drain

Figures 3
POTENTIAL Vp OF VERTICAL GATE LINE

Figures 5
POTENTIAL Vp OF VERTICAL GATE LINE

Figures 7
POTENTIAL Vp OF VERTICAL GATE LINE

Figures 9
POTENTIAL Vp OF VERTICAL GATE LINE

Figures 11
POTENTIAL Vp OF VERTICAL GATE LINE

Fig. 1

第 1 図

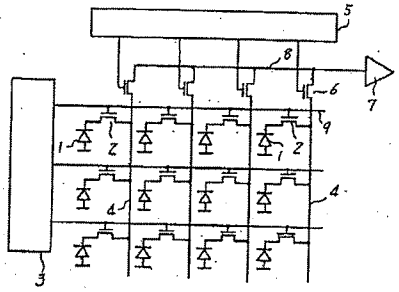


Fig. 2

第 2 図

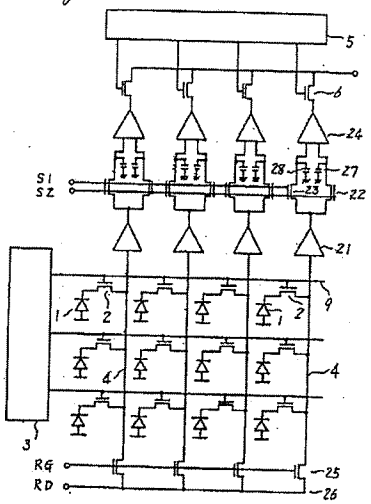


Fig. 3

第 3 図

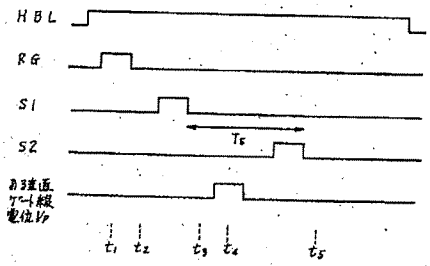
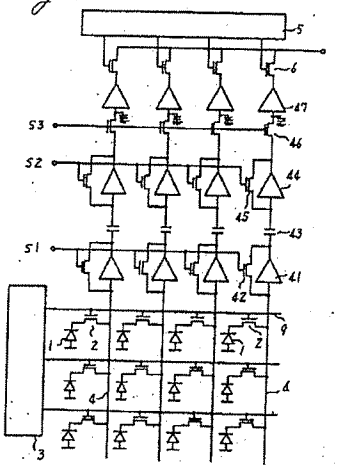
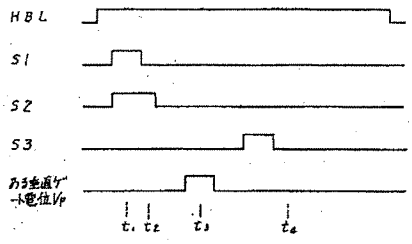


Fig. 4

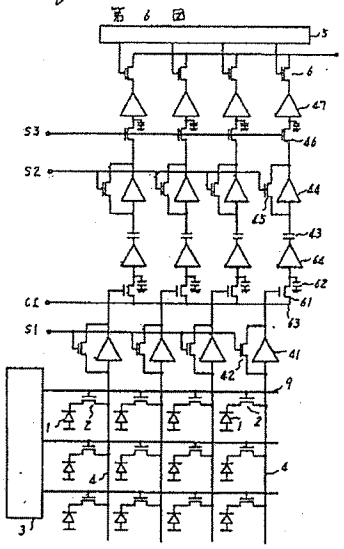
第 4 図



第 5 図　Fig. 5



第 6 図



第 7 図　Fig. 7

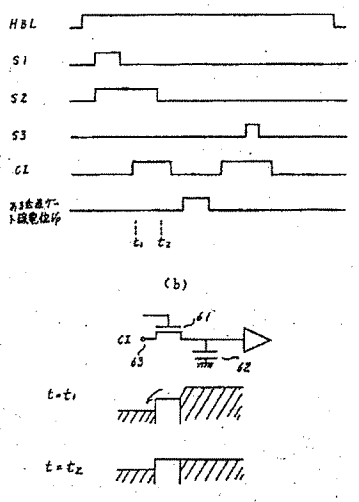
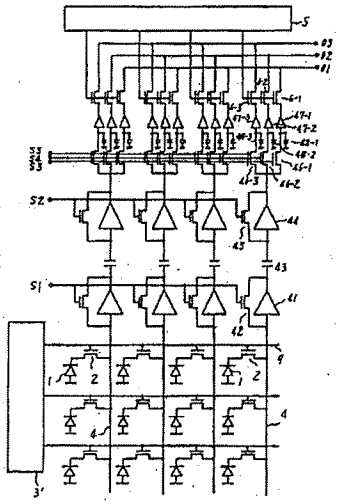
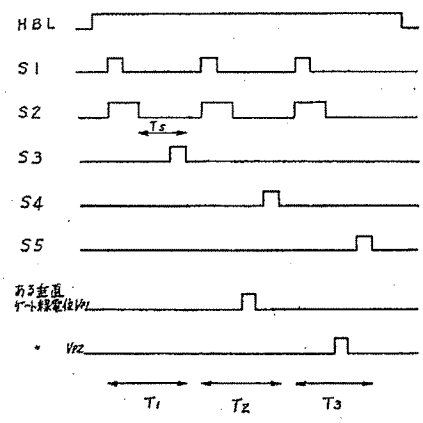


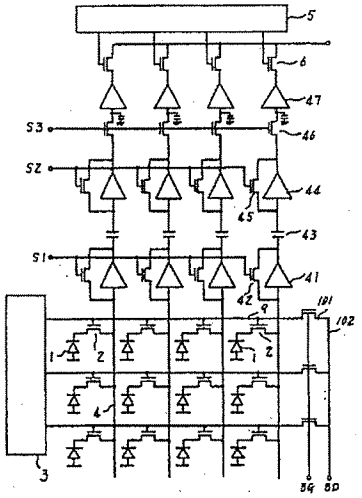
Fig. 8　第 8 図



第 9 図 Fig. 9



第 10 図 Fig. 10



第 11 図 Fig. 11